IN THE CLAIMS

1 (Original). A method comprising:

receiving a data frame of a first size;

demultiplexing said data frame;

writing blocks of the demultiplexed data frame at the first size into a register;

reading blocks of a second size, different from said first size, from said register; and

multiplexing said blocks to form an output data frame of the second size.

2 (Original). The method of claim 1 wherein receiving a data frame of a first size includes receiving a 64-bit data frame.

3 (Original). The method of claim 2 wherein demultiplexing said data frame includes providing said data frame to a one to thirty-three demultiplexer.

4 (Original). The method of claim 3 wherein writing blocks of the demultiplexed data frame at the first size includes writing blocks of 64-bits to a register.

5 (Original). The method of claim 4 wherein writing the blocks into a register include writing 2,112 bits into a register.

6 (Original). The method of claim 5 including controlling a write pointer at a frequency of approximately 161 MegaHertz.

7 (Original). The method of claim 5 wherein reading blocks of the second size includes reading blocks of sixty-six bits from said register.

8 (Original). The method of claim 7 including controlling a read pointer at a frequency of approximately 156 MegaHertz.

9 (Original). The method of claim 7 wherein multiplexing said blocks to form an output data frame of a second size includes forming an output data frame by using a thirty-two to one multiplexer.

10 (Original). The method of claim 1 including converting a sixty-four bit data frame to a sixty-six bit data frame.

11 (Original). A device comprising:

a demultiplexer coupled to receive a data frame of a first size;

a register coupled to receive data from said demultiplexer; and

a multiplexer coupled to the output of said register, the output of said multiplexer being a data frame of a second size different from said first size.

12 (Original). The device of claim 11 including a first counter to control the writing of data from said demultiplexer to said register.

13 (Original). The device of claim 11 including a second counter to control the reading of data from said register to said multiplexer.

14 (Original). The device of claim 11 wherein data is written to said register at approximately 161 MegaHertz and data is read from said multiplexer at approximately 156 MegaHertz.

15 (Original). The device of claim 11 wherein said demultiplexer receives a data frame of 64-bits and said multiplexer outputs a data frame of 66-bits.

16 (Original). The device of claim 11 wherein said demultiplexer is a one to thirty-three demultiplexer.

17 (Original). The device of claim 11 wherein said multiplexer is a thirty-two to one multiplexer.

18 (Original). The device of claim 11 wherein said demultiplexer writes data to said register in 64-bit blocks.

19 (Original). The device of claim 11 wherein said multiplexer reads data from said register in 66-bit blocks.

20 (Original). The device of claim 11 wherein said demultiplexer writes data in blocks of a first size to said register and said multiplexer reads data in blocks of a second size, different from said first size, from said register.

21 (Original). The device of claim 11 wherein said device is part of a physical coding sublayer.

22 (Original). The device of claim 21 wherein said device is part of a receiver in a fiber optic network.

Claims 23-55 (Canceled).